FIG. 1

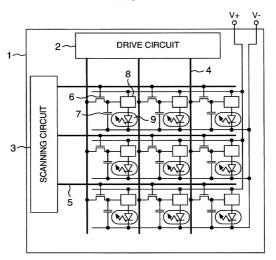
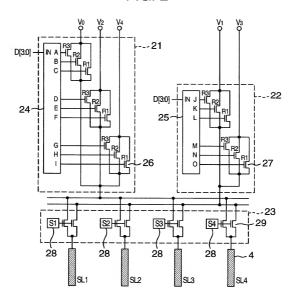


FIG. 2



21, 22 D/A CONVERSION CIRCUIT 23 SAMPLING CIRCUIT 24, 25, 28 CONTROL CIRCUIT 26, 27, 29 THIN-FILM TRANSISTOR SL1 TO SL4 SIGNAL LINE

FIG. 3A

IN	Α	В	С	D	E	F	G	Н	1
0	1	1	1	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0
5	0	0	0	1	1	0	0	0	0
6	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	1	0	0	0
8	0	0	0	1	1	1	0	0	0
9	0	0	0	0	0	1	0	0	0
10	0	0	0	0	0	0	0	0	0
11	0	0	0	1	1	0	0	0	0
12	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	1	0	0
14	0	0	0	0	0	0	0	1	0
15	0	0	0	0	0	0	0	0	1

FIG. 3B

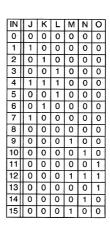


FIG. 4

IN	GENERATION OF VSL		
0	Vn		
1	Vn Vn+1		
2	Vn Vn+1		
3	Vn Vn+1 9 R3 R5 R5 VSL= (Vn+3Vn+1)/4		

FIG. 5

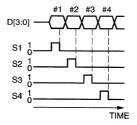


FIG. 6

D[3:0]	V _{SL}		
0	V _o		
1	$(3V_0 + V_1)/4$		
2	$(V_0+V_1)/2$		
3	$(V_0+3V_1)/4$		
4	V ₁		
5	$(3V_1+V_2)/4$		
6	$(V_1 + V_2)/2$		
7	$(V_1 + 3V_2) / 4$		
8	V ₂		
9	$(3V_2 + V_3)/4$		
10	$(V_2+V_3)/2$		
11	$(V_2 + 3V_3) / 4$		
12	V ₃		
13	$(3V_3 + V_4)/4$		
14	$(V_3+V_4)/2$		
15	$(V_3 + 3V_4)/4$		

FIG. 7

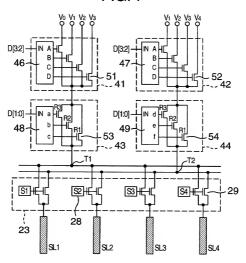


FIG. 8A

FIG. 8B

FIG. 8C

IN	A	В	С	D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

İ	IN	а	b	С
	0	1	1	1
	1	0	0	1
	2	0	1	0
	3	1	0	0

IN	d	е	f
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1

FIG. 9

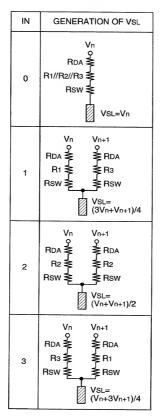


FIG. 10

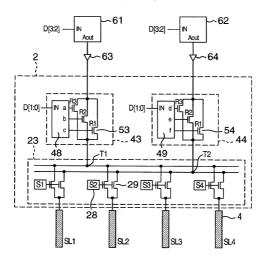
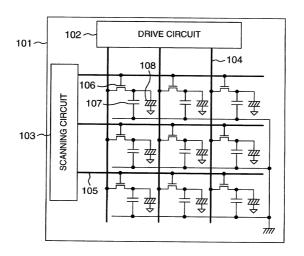


FIG. 11

IN	61 Aout	62 Aout
0	V0	V1
1	V1	V2
2	V2	V3
3	V3	V4

FIG. 12



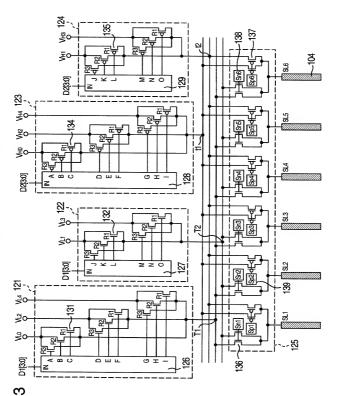


FIG. 13

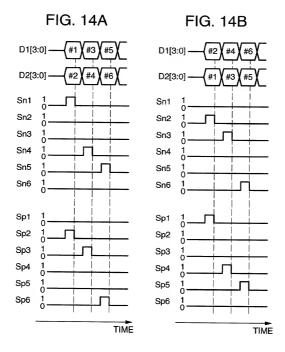


FIG. 15

D[3:0]	(a)	(b)
0	V _{H0}	V _{LO}
1	(3V _{H0} +V _{H1})/4	(3V _{L0} +V _{L1})/4
2	(V _{H0} +V _{H1})/2	$(V_{L0} + V_{L1})/2$
3	(V _{H0} +3V _{H1})/4	$(V_{L0} + 3V_{L1})/4$
4	V _{H1}	V _{L1}
5	(3V _{H1} +V _{H2})/4	$(3V_{L1} + V_{L2})/4$
6	$(V_{H1} + V_{H2})/2$	$(V_{L1} + V_{L2})/2$
7	$(V_{H1} + 3V_{H2})/4$	$(V_{L1} + 3V_{L2})/4$
8	V _{H2}	V _{L2}
9	(3V _{H2} +V _{H3})/4	$(3V_{L2} + V_{L3})/4$
10	(V _{H2} +V _{H3})/2	$(V_{L2} + V_{L3})/2$
11	$(V_{H2} + 3V_{H3}) / 4$	$(V_{L2} + 3V_{L3}) / 4$
12	V _{H3}	V _{L3}
13	(3V _{H3} +V _{H4})/4	$(3V_{L3} + V_{L4})/4$
14	$(V_{H3} + V_{H4})/2$	$(V_{L3} + V_{L4})/2$
15	(V _{H3} +3V _{H4})/4	(V _{L3} +3V _{L4})/4

FIG. 18

IN	171About	172About	173About	174About
0	VL0	VL1	VH0	VH1
1	VL1	VL2	VH1	VH2
2	VL2	VL3	VH2	VH3
3	VL3	VL4	VH3	VH4

FIG. 16

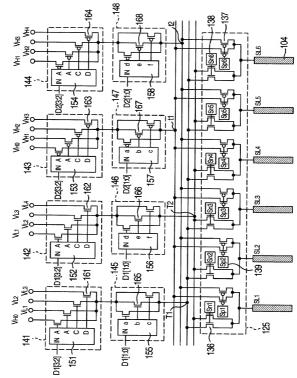


FIG. 17

CHECK!

